CLAIMS

What is claimed is:

1. A method comprising:

selecting a phase threshold value,

receiving a plurality of sequenced buffers,

determining a distance between centers of at least two consecutive histogram bins,

comparing the distance with said selected threshold value, and

determining major execution phases of an executable process based on the comparison.

2. The method of claim 1, said plurality of sequenced buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.

3. The method of claim1, further comprising:

determining a plurality of branch addresses representing a branch trace buffer,

determining a plurality of consecutive branch addresses representing the branch trace buffer,

determining a stable phase histogram for the plurality of consecutive branch addresses, and

determining a plurality of equally spaced and non-overlapping histogram bins for all possible branch addresses.

4. The method of claim 1, where a result of said determining major execution phases to signal a requisite for dynamically compiling executable code to optimize said executable code.

5. The method of claim 1, further comprising:

determining whether the at least two consecutive histogram bins are in the same phase.

6. The method of claim 5, said at least two consecutive histograms are in the same phase if said distance is less than one of equal to and less than said selected phase threshold value.

7. An apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

selecting a phase threshold value,

receiving a plurality of sequenced buffers,

determining a plurality of branch addresses representing a branch trace buffer,

determining a distance between centers of at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping, and

comparing the distance with said selected threshold value.

8. The apparatus of claim 7, further including instructions which, when executed by a machine, cause the machine to perform operations including:

determining a plurality of consecutive branch addresses representing the branch trace buffer,

determining a stable phase histogram for the plurality of consecutive branch addresses,

determining a plurality of equally spaced and non-overlapping histogram bins for all possible branch addresses, and

determining major execution phases of an executable process based on the comparison.

9. The apparatus of claim 8, wherein said determining major execution phases is dynamic at a predetermined periodic rate.

10. The apparatus of claim 8, wherein said determining major execution phases is manually commenced.

11. The apparatus of claim 7, said plurality of sequenced buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.

12. The apparatus of claim 7, where a result of said determining major execution phases instruction to signal a requisite for dynamically compiling executable code to optimize said executable code.

13. The apparatus of claim 7, further including instructions which, when executed by a machine, cause the machine to perform operations including:

determining whether the at least two consecutive histogram bins are in the same phase.

14. The apparatus of claim 13, said at least two consecutive histograms are in the same phase if said distance is less than one of equal to and less than said selected phase threshold value.

15. A system comprising:

a processor coupled to one of a main memory and a cache memory,

at least one process to communicate with said memory, and a

phase detector to determine major execution phases of said at least one process.

16. The system of claim 15, said determined major execution phases to determine when to re-optimize said process.

17. The system of claim 15, said phase detector including a receiver to

receive a plurality of sequenced buffers,

wherein said phase detector to determine a plurality of branch addresses representing a branch trace buffer,

determine a distance between centers of at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping, and

compare the distance with a predetermined threshold value.

18. The system of claim 17, said phase detector having logic to:

determine a plurality of consecutive branch addresses representing the branch trace buffer,

determine a stable phase histogram for the plurality of consecutive branch addresses, and

determine a plurality of equally spaced and non-overlapping histogram bins for all possible branch addresses.

19. The system of claim 15, wherein said phase detector having logic to determine major execution phases dynamically at a predetermined periodic rate.

20. The system of claim 17, said plurality of sequenced buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.

21. A system comprising:

a first device having a first processor coupled to a first memory and at least one process to communicate with said first memory, and

a second device having a second processor coupled to a second memory and at least another process to communicate with said second memory,

wherein a phase detector process operating in one of said first processor and said second processor to determine major execution phases of one of said one process and said another process within one of said first device and said second device.

22. The system of claim 21, said major execution phases to determine when to re-optimize said one process and said another process.

23. The system of claim 21, said phase detector having logic to:

receive a plurality of sequenced buffers,

determine a plurality of branch addresses representing a branch trace buffer,

determine a distance between centers of at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping, and

compare the distance with a predetermined threshold value.

24. The system of claim 23, said phase detector having logic to:

determine a plurality of consecutive branch addresses representing the branch trace buffer,

determine a stable phase histogram for the plurality of consecutive branch addresses, and

determine a plurality of equally spaced and non-overlapping histogram bins for all possible branch addresses.

25. The system of claim 21, wherein said phase detector having logic to determine major execution phases dynamically at a predetermined periodic rate.

26. The system of claim 23, said plurality of sequenced buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.